**WHAT IS CLAIMED IS:**

1. A method for testing memory of an information handling system, the method comprising:

initiating startup of the information handling system;

determining that a memory test is required;

generating test data according to one or more test routines with the information handling system CPU, the CPU having SIMD registers;

communicating the test data to and from a predetermined portion of the memory through the SIMD registers; and

passing the memory test if test data communicated from the memory has a predetermined relationship with the generated test data.

2. The method of Claim 1 further comprising:

using CPU 64-bit MMX registers for temporary storage of the test data.

3. The method of Claim 1 wherein the predetermined portion comprises at least one Mbyte, the method further comprising:

incrementing the memory address of the predetermined portion by the at least one Mbyte;

repeating the generating, communicating and passing for the incremented portion of memory; and

repeating the incrementing until each portion of the memory passed the memory test.

4. The method of Claim 3 wherein determining an memory test is required further comprises setting the gate A20 to support the memory test before the generating of test data, the method further comprising:

maintaining the gate A20 setting through each incrementing; and

resetting the gate A20 after each portion of the memory passes the memory test.

5. The method of Claim 3 wherein determining a memory test is required further comprises entering the protected mode before the generating of test data, the method further comprising:

maintaining the protected mode through each incrementing; and

exiting the protected mode after each portion of the memory passes the memory test.

6. The method of Claim 1 wherein generating the test data further comprises:

using ADD and SUB instructions; and

avoiding INC and DEC instructions.

7. The method of Claim 6 wherein generating the test data further comprises:

generating test data with a boundary test routine; and

generating test data with a stuck bit test routine.

8. The method of Claim 7 wherein generating test data further comprises executing 32-bit code on the CPU.

9. The method of Claim 1 wherein generating test data further comprises:

using the MOVNTDQ instruction on the CPU to move test data in the memory in 128-bit increments.

10. An information handling system comprising:

a CPU operable to perform instructions;

random access memory interfaced with the CPU and operable to store information;

a firmware operable to startup the CPU to an operational state, the firmware further operable to coordinate execution of instructions by the CPU to test the memory, the instructions comprising 32-bit code to:

initiate a memory test during startup;

generate test data to write to and read from the random access memory using 128-bit SIMD registers and the MOVNTDQ instruction;

apply the test data iteratively to predetermined sized portions of the random access memory until the test data has been written to and read from each portion; and

passing the memory test if test data read from the random access memory has a predetermined relationship with the test data written to the random access memory.

11. The information handling system of Claim 10 wherein the instructions to generate test data further comprise instructions to:

perform a walking 1s and 0s routine; and

perform a multi-pattern routine.

12. The information handling system of Claim 11 wherein the instructions to generate test data comprise ADD and SUB instructions and lack INC and DEC instructions.

13. The information handling system of Claim 12 wherein the portions are at least one Mbyte in size.

14. The information handling system of Claim 10 further comprising instructions to:

set gate A20 before generating the test data;

maintain the gate A20 setting through each iterative application of the test data to the portions; and

reset gate A20 upon completion of all iterative applications of the test data.

15. The information handling system of Claim 10 further comprising instructions to:

enter a protected mode before generating the test data;

maintain the protected mode through each iterative application of the test data to the portions; and

exiting the protected mode upon completion of all iterative applications of the test data.

16. The information handling system of Claim 10 further comprising instructions to use 64-bit MMX registers of the CPU for temporary storage of test data.

17. A method for testing memory at boot of an information handling system, the method comprising:

initiating a memory test during POST;

generating test data to write to and read from the memory using 128-bit SIMD registers and the MOVNTDQ instruction;

applying the test data iteratively to predetermined sized portions of the memory until the test data has been written to and read from each portion; and

passing the memory test if test data read from the random access memory has a predetermined relationship with the test data written to the random access memory.

18. The method of Claim 17 further comprising:

setting gate A20 and entering the protected mode before generating the test data;

maintaining the gate A20 setting and protected mode through each iterative application of the test data to the portions; and

resetting gate A20 and exiting the protective mode upon completion of the iterative applications of the test data to each portion of the memory.

19. The method of Claim 18 wherein generating test data further comprises:

executing a walking 1s and 0s test routine; and

executing a multi-pattern test routine.

20. The method of Claim 19 wherein generating test data further comprises executing ADD and SUB instructions.